exact quotes from the claim, but reasonably close), on the grounds that:

> "a preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone."

Applicant respectfully submits that the body of claims 1 and 2 as previously presented did depend on the preamble for completeness. The reference in the body to "the graph" clearly references a term defined only in the preamble, and specifies an environment in which the claims method operates; the body only makes sense with reference to that term. Nevertheless, in order to clarify the claims, Applicant has amended claims 1 and 2 to positively recite comparable terms in the body of those claims.

The §103 Rejection

The Examiner has rejected claims 1-2 under 35 U.S.C. §103(a) as being obvious over Benner et al. ('216) in view of Tsuchida et al. ('059). Applicant respectfully traverses this rejection.

As noted previously, Benner teaches a method for more efficiently operating the hardware of a parallel computing system by employing sequenced communications. Benner has no teachings about applications expressed as a graph of vertices (the Examiner's prior citation to FIG. 4 of Benner mischaracterizes Benner's teachings – FIG. 4 is a diagram of a "4 dimension hypercube structure for a parallel computer", not a graph as described in the present application). Benner teaches

nothing about accessing and analyzing the capacity of such an application executing on a parallel processing system. Benner teaches nothing about creating a performance description of each vertex in the graph and determining an execution time for each vertex in the graph (the Examiner's citation to FIG. 3 of Benner mischaracterizes Benner's teachings – FIG. 3 shows "use of overlap communications" to carefully order reads and writes of memory locations; see col. 8, lines 12-35). Thus, Benner is not even applicable art, let alone art that suggests features of the invention as now claimed.

While Tsuchida does suggest that the processing time of each processing node does vary with the "number" (amount) of data being processed, that is neither surprising nor relevant. Tsuchida not only has no teaching about applications expressed as a graph of vertices, Tsuchida has no teaching about any method or system for analyzing the capacity of such an application executing on a parallel processing system. Thus, Tsuchida is not even applicable art, let alone art that suggests features invention as claimed.
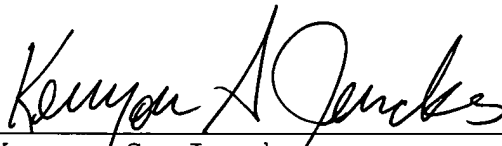
Even in combination, Benner and Tsuchida fail to teach or suggest the invention as claimed. One of ordinary skill in the art, fairly reading Benner and Tsuchida, would have no idea how to analyze the capacity of an application. The amendment of claim 1 effectively imports limitations from the claim preamble into the claim body that recite elements clearly not taught in the cited references, alone or in combination. In particular, these references fail to teach or suggest <u>accessing an application for processing designated data records on a parallel processing system, such application being expressed as a graph of vertices</u>, and then creating a description of the sizes of data records throughout the graph; creating a performance

description of each vertex·in the graph; determining an execution time for each vertex in the graph; determining counts of data records assigned to corresponding vertices in the graph; and creating outputting a description of the total execution time and performance of the parallel processing system based on the determined execution time and counts of data records.

Applicant submits that all of the claims are now in condition for allowance, which action is requested. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 11/21/00

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